Abstract

A clock synchronization circuit (200, Figure 2) includes a signal selector (202), phase detector (204), and delay line (206). The signal selector compares an external clock signal (220) and a feedback signal (222) to evaluate the jitter present in the external clock signal. When the jitter falls within an acceptable range, the circuit operates in DLL mode. In DLL mode, the external clock signal is provided to the delay line, and the delayed external signal is output (224) from the circuit. If the jitter falls outside the acceptable range and the circuit is locked, the circuit is switched to PLL mode. In PLL mode, a clock signal based on the feedback signal is provided to the delay line, and the delayed feedback signal is output from the circuit. The PLL mode is only allowed to operate briefly before switching the circuit back into DLL mode.